1. (currently amended) A method of generating a test pattern for an integrated circuit set in m scan flip-flops (m indicates any natural number) when m outputs from a logical circuit are applied to m output terminals through m scan flip-flops and m output buffers, comprising:

a first process of counting the total number of output buffers, whose output values change, when said m scan flip-flops output an input pattern to said m output ~~buffers as input patterns;~~ buffers;

a second process of checking a total noise value generated from all output buffers counted in said first process based on a noise value defined for each of said m output buffers;

a third process of selecting output buffers from the total output buffers counted in said first process such that said total noise value check can be within an allowable noise value; and

a fourth process of outputting the test pattern obtained by amending the input pattern such that only the output buffers selected in said third process can change output values.

2. (currently amended) A method of generating a test pattern for an integrated circuit set in m scan flip-flops (m indicates any natural number) when m outputs from a logical circuit are applied to m output terminals through m scan flip-flops and m output buffers, and ~~when~~ n (n indicates any natural number) outputs from the logical circuit are applied to n output terminals through n output buffers, and without passing through said m scan flip-~~flips,~~ flops, comprising:

a first process of counting the total number of output buffers, whose output values change, when said m scan flip-flops output ~~patterns~~ an input pattern to said m output ~~buffers as input patterns;~~ buffers;

a second process of checking a first sum of noise value generated from all output buffers counted in said first process based on a noise value defined for each of said m output buffers, a second sum of noise value generated from said n output buffers when output values of said n output buffers are changed based on a noise value defined for each of said n output buffers, and total noise value of said first and second sum of noise value;

a third process of selecting output buffers from the total output buffers counted in said first process such that said total noise value can be within an allowable noise value; and

a fourth process of outputting the test pattern obtained by amending the input pattern such that only the output buffers selected in said third process can change output values.

3. (previously amended) The method according to claim 1, wherein

said second through fourth processes are repeated on said output buffer not selected in said third process when said fourth process is completed.

4. (currently amended) A method of generating a test pattern for an integrated circuit set in m scan flip-flops (m indicates any natural number) when m outputs from a logical circuit are applied to m output terminals through m scan flip-flops and m output buffers, comprising:

within ~~a noise~~ an allowable noise value, said total noise value being checked based on a noise value defined for each of said output buffers;

a second process of selecting one group from among groups generated in said first process;

a third process of outputting as the test pattern a pattern in which only output values of output buffers belonging to the group selected by said second process changes when said m scan flip-flops output input patterns to said m output buffers, and output values of output buffers belonging to groups not selected in said second process remain unchanged; and

a fourth process of repeating said second and third processes on the groups not selected in said second process when said third process is completed.